## CLAIMS

What is claimed is:

1. A method for detecting biphase encoded data comprising:

receiving a biphase encoded signal, the biphase encoded signal characterized as including unit bit cells each having a logic value encoded as a mid-symbol signal transition between a first half-symbol signal component and a second half-symbol signal component;

demodulating the first and second half-symbol signal components of a unit bit cell; and

generating a difference signal corresponding to the difference between the demodulated first and second half-symbol components, such that the difference signal may be utilized to determine the logic value of the unit bit cell.

2. The method of claim 1, further comprising detecting the logic value of the received unit bit cell by comparing the difference signal with a validity threshold value.

3. The method of claim 1, wherein the received biphase encoded signal is a Manchester encoded signal.

4. The method of claim 1, wherein said biphase encoded signal is modulated as amplitude shift keyed, frequency shift keyed, or phase shift keyed.

5. The method of claim 1, wherein said step of generating a difference signal comprises subtracting the demodulated first half-symbol signal component from the demodulated second half-symbol signal component.

6. The method of claim 1, wherein said step of generating a difference signal comprises subtracting the demodulated second half-symbol signal component from the demodulated first half-symbol signal component.

7. The method of claim 1, said demodulating step comprising demodulating the first and second half-symbol signal components of the unit bit cell over sequential half symbol clock periods.

8. The method of claim 1, wherein said demodulating step further comprising correlating the first and second half-symbol signal components of the unit bit cell.

9. The method of claim 8, wherein said correlating step comprises separating the first and second half-symbol signal components of the unit bit cell.

10. The method of claim 8, said demodulating step further comprising integrating the correlated first and second half-symbol signal components of the unit bit cell.

11. A biphase code detector for detecting biphase encoded data comprising:

a receiver that receives a biphase encoded signal, wherein the biphase encoded signal is characterized as including unit bit cells each having a logic value encoded as a mid-symbol transition between a first half-symbol signal component and a second half-symbol signal component;

a demodulator that demodulates the first and second half-symbol components; and

a half-symbol differentiator that generates a difference signal corresponding to the difference between the demodulated first and second half-symbol components, such that the difference signal may be utilized to determine the logic value of the unit bit cell.

12. The system of claim 11, further comprising an output detector that compares the difference signal with a validity threshold value to determine the logic value of the received unit bit cell.

13. The system of claim 11, wherein said half-symbol differentiator comprises a subtractor.

14. The system of claim 11, said demodulator further comprising means for correlating the first and second half-symbol components over sequential half-symbol clock periods.

15. The system of claim 14, wherein said correlation means comprises a first and a second integrate and dump circuit.

16. The system of claim 15, wherein said correlation means further comprises:

means for separating and passing the first half-symbol component to either the first or second integrate and dump circuit; and

means for separating and passing the second half-symbol component to the other of the first or second integrate and dump circuits.

17. The system of claim 16, wherein said means for separating and passing comprise correlation multipliers.